CLAIMS

1. A process for producing a semiconductor integrated circuit device, which comprises a step of forming a first conduction type well in a silicon substrate; a step of forming a first pattern to act as floating gates on the silicon substrate through a first insulator film; a step of forming second conduction type semiconductor regions to act as sources/drains in the well; a step of forming a second insulator film covering the first pattern; a step of forming third gates in gaps formed in the first pattern through the second insulator film; a step of forming control gates on the upper surfaces of the floating gates and the third gates, the height of the upper surfaces of the third gates formed being lower than the height of the upper surface of the first pattern.

2. A process according to Claim 1, wherein the third gates are formed by any one of a first method of forming a polysilicon film completely filling the gaps, and then dry etching the polysilicon film, a second method of forming a polysilicon film completely filling the gaps, and then polishing the polysilicon film by chemical mechanical polishing, followed by dry etching, and a third method of forming a polysilicon film completely filling the gaps, then polishing the polysilicon film by chemical mechanical polishing, oxidizing the surface of the polysilicon film and selectively removing the oxidized parts.

3. A process according to Claim 1, wherein the third gates are formed by any one of a first method of forming a polysilicon film so as not to completely fill the gaps, then forming a photo resist film to fill the gap, and dry etching the photo resist film and the polysilicon film, a second method of forming a polysilicon film so as not to completely fill the gaps, then polishing the polysilicon film by chemical mechanical polishing, forming a photo resist to fill the gaps and dry etching the photo resist film and the polysilicon film, and a third method of forming a polysilicon film so as not to completely fill the gaps, then depositing a silicon oxide film to fill the gaps, polishing the silicon oxide film and the polysilicon film by chemical mechanical polishing, selectively removing the silicon oxide film in the gaps, forming a photo resist film to fill the gaps and dry etching the photo resist film and the polysilicon film.

4. A process according to Claim 3, wherein the dry etching of the photo resist and the polysilicon film is carried out at substantially equal etching speeds.

5. A process according to Claim 1, wherein the third gates are formed by a method of forming a polysilicon film so as not to completely fill the gaps, then forming a silicon oxide film on the polysilicon film, polishing the silicon oxide film and the polysilicon film by chemical mechanical polishing, dry

etching the polysilicon film and removing the silicon oxide film.

6. A process according to any one of Claims 3 to 5, wherein the thickness of the polysilicon film is made smaller than that of the first pattern to act as the floating gates.

7. A process for producing a semiconductor integrated circuit device, which comprises a step of forming a first conduction type well in a silicon substrate; a step of forming third gates on the silicon substrate through a second insulator film; a step of forming second conduction type semiconductor regions to act as sources/drains in the well; a step of forming a first insulator film covering the third gates; a step of forming a first pattern to act as floating gates in gaps formed between the third gates through the first insulator film; and a step of forming control gates on the upper surfaces of the floating gates and the third gates, the height of the upper surfaces of the third gates thus formed being made lower than that of the upper surface of the first pattern.

8. A process according to Claim 7, wherein the first pattern is formed by any one of a first method of forming a polysilicon film to completely fill the gaps, and then dry etching the polysilicon film, a second method of forming a polysilicon film to completely fill the gaps and then polishing the polysilicon film by chemical mechanical polishing, followed by dry etching;

a third method of forming a polysilicon film so as not to completely fill the gaps and then polishing the polysilicon film by chemical mechanical polishing, a fourth method of forming a polysilicon film so as not to completely fill the gaps, then forming a photo resist film to fill the gaps and dry etching the photo resist film and the polysilicon film, and a fifth method of forming a polysilicon film so as not to completely fill the gaps, then depositing a silicon oxide film to fill the gaps and polishing the silicon oxide film and the polysilicon film by chemical mechanical polishing.

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9. A process according to any one of Claims 1 to 8, wherein the third gates are self-aligned to the floating gates.

10. A process according to any one of Claims 1 to 8, wherein the floating gates are self-aligned to the third gates.

11. A semiconductor integrated circuit device, which comprises a first conduction type well formed on the main surface of a semiconductor substrate, second conduction type semiconductor regions formed in the well, first gates formed on the semiconductor substrate through a first insulator film, second gates formed on the first gates through a second insulator film and third gates formed through the first gates and a third insulator film, the third gates being formed to fill gaps between the first gates and the height of the

surfaces of the third gates being made lower than that of the surfaces of the first gates.

12. A semiconductor integrated circuit device according to Claim 11, wherein the third gates are in any one of a first structure of erase gates, a second structure of gates controlling split channels, and a third structure having both functions of erase gates and gates controlling split channels.

13. A semiconductor integrated circuit device according to Claim 11 or 12, wherein the third insulator film is a nitrogen-introduced silicon oxide film.

ADDITIONAL CLAIMS 14-39

14. A process for producing a semiconductor integrated circuit device, which comprises

a step of forming a first conduction type well in a silicon substrate,

a step of forming a first pattern which is to become floating gates through a first insulator film on the semiconductor substrate,

a step of forming second conduction type semiconductor regions to act as sources/drains in the well,

a step of forming a second insulator film covering at least side faces of the first pattern and the semiconductor substrate surface between each first pattern,

a step of forming third gates in individual gaps formed by the first pattern so as to make individual side faces of the third gates opposed to side faces of neighboring first pattern through the second insulator film and to make bottom sides of the third gates opposed to a surface of the semiconductor substrate through the second insulator film by depositing a third gate material film, followed by removing the material film above each first pattern, and

a step of forming the floating gates and forming control gates on the third gates.

15. A process for producing a semiconductor integrated circuit device according to claim 14, wherein the upper ends of side faces of the third gates are formed lower than the upper ends of side faces of the first pattern which is to become the floating gates opposed to the side faces of the third gates.

16. A process for producing a semiconductor integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film for completely filling the gaps, and dry etching

the polycrystalline silicon film.

17. A process for producing a semiconductor integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film for completely filling the gaps, polishing the polycrystalline silicon film by a chemical mechanical polishing method, followed by dry etching.

18. A process for producing a semiconductor integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film for completely filling the gaps, polishing the polycrystalline silicon film by a chemical mechanical polishing method, oxidizing a surface of the polycrystalline silicon film, and selectively removing the oxidized portion thus obtained.

19. A process for producing a semiconductor integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, forming a photo resist film for filling the gaps, and subjecting the photo resist film and the polycrystalline silicon film to dry etching.

20. A process for producing a semiconductor integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, polishing the polycrystalline silicon film by a chemical mechanical polishing method, forming a photo resist film for filling the gaps, and subjecting the photo resist film and the polycrystalline silicon film to dry etching.

21. A process for producing a semiconductor

integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, depositing a silicon oxide film for filling the gaps, polishing the silicon oxide film and the polycrystalline silicon film by a chemical mechanical polishing method, selectively removing the silicon oxide film in the gaps, forming a photo resist film for filling the gaps, and subjecting the photo resist film and the polycrystalline silicon film to dry etching.

22. A process for producing a semiconductor integrated circuit device according to any one of claims 19 to 21, wherein the dry etching of the photo resist film and that of the polycrystalline silicon film are conducted at almost the same etching speed.

23. A process for producing a semiconductor integrated circuit device according to claim 15, wherein the third gates are obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, forming a silicon oxide film on the polycrystalline silicon film, polishing the silicon oxide film and the polycrystalline silicon film by a chemical mechanical polishing method, dry etching the polycrystalline silicon film, and removing the silicon oxide film.

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24. A process for producing a semiconductor integrated circuit device according to any one of claims 19 to 23, wherein the polycrystalline silicon film has a film thickness thinner than that of the first pattern which becomes the floating gates.

25. A process for producing a semiconductor integrated circuit device, which comprises a step of forming a first conduction type well

in a silicon substrate,

a step of forming a plurality of third gates through a second insulator film on the semiconductor substrate,

a step of forming second conduction type semiconductor regions to act as sources/drains in the well,

a step of forming a first insulator film covering at least side faces of the third gates and the semiconductor substrate surface between each third gates,

a step of forming a first pattern which is to become floating gates in individual gaps formed by the third gates so as to make individual side faces of the first pattern opposed to side faces of neighboring third gates through the first insulator film and to make a bottom side of the first pattern opposed to a surface of the semiconductor substrate through the first insulator film by depositing a floating gate material film, followed by removing the material film above each third gate, and

a step of forming the floating gates and forming control gates on the third gates.

26. A process for producing a semiconductor integrated circuit device according to claim 25, wherein the upper ends of side faces of the third gates are formed lower than the upper end of side face of the first pattern which is to become the floating gates opposed to the side faces of the third gates.

27. A process for producing a semiconductor integrated circuit device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline silicon film for completely filling the gaps, and dry etching the polycrystalline silicon film.

28. A process for producing a semiconductor integrated circuit device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline

silicon film for compl tely filling the gaps, polishing the polycrystalline silicon film by a chemical mechanical polishing method, followed by dry etching.

29. A process for producing a semiconductor integrated circuit device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, and polishing the polycrystalline silicon film by a chemical mechanical polishing method.

30. A process for producing a semiconductor integrated circuit device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, forming a photo resist film for filling the gaps, and subjecting the photo resist film and the polycrystalline silicon film to dry etching.

31. A process for producing a semiconductor integrated circuit device according to claim 26, wherein the first pattern is obtained by forming a polycrystalline silicon film so as not to completely fill the gaps, depositing a silicon oxide film for filling the gaps, and polishing the silicon oxide film and the polycrystalline silicon film by a chemical mechanical polishing method.

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32. A process for producing a semiconductor integrated circuit device according to any one of claims 14 to 31, wherein the third gates are formed as self-aligned to the floating gates.

33. A process for producing a semiconductor integrated circuit device according to any one of claims 14 to 31, wherein the floating gates are formed as self-aligned to the third gates.

34. A semiconductor integrated circuit device comprising a first conduction type well formed on a major surface of a semiconductor substrate, second conduction type semiconductor regions formed in the well, first gates formed on the semiconductor substrate through a first insulator film, second gates formed on the first gates through a second insulator film, and third gates formed through the first gates and a third insulator film, wherein the third gates are formed by filling gaps in the first gates so as to make side faces of the third gates opposed to neighboring side faces of the first gates through the third insulator film and extended in an almost vertical direction to the direction of extended second gates.

35. A semiconductor integrated circuit device according to claim 34, wherein the third gates have upper ends of side faces lower than upper ends of side faces of the first gates opposed to the side faces of the third gates.

36. A semiconductor integrated circuit device according to claim 35, wherein the third gates are erase gates.

37. A semiconductor integrated circuit device according to claim 35, wherein the third gates are gates for controlling split channels.

38. A semiconductor integrated circuit device according to claim 35, wherein the third gates have functions of both erase gates and gates for controlling split channels.

39. A semiconductor integrated circuit device according to any one of claims 35 to 38, wherein the third insulator film is a nitrogen-introduced silicon oxide film.

Add A4